REMARKS

Claims 19-44 are pending.

Claims 19-44 stand rejected.

Claims 39-42 have been amended.

No new matter has been added.

Claims 19-44 are hereby submitted for reconsideration.

In paragraph 2 of the Office Action, the Examiner has objected to the abstract for being excessive in length. Applicants have amended the abstract accordingly and respectfully request that this objection be withdrawn.

In paragraphs 4 and 5 of the Office Action, the Examiner has rejected claims 39-42 under 35 U.S.C. § 112 as being unpatentable for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Applicants have amended the claims accordingly to clarify the scope of the claims and respectfully request that the rejection of these claims be withdrawn.

In particular, claims 39 and 40 now recite that the data streamer schedule simultaneous data transfers include *the interface unit* which is capable of controlling the external I/O devices, and *a memory controller* which is capable of controlling an external memory. Both the memory controller 124 and the interface unit 202 are both located within the multimedia processor 100 as seen in Fig. 1A. Additionally, the relevant portion of claim 40 has been deleted and proper

F

antecedent basis has been provided for the final element of claim 42.

In paragraph 6 of the Office Action the Examiner has rejected claims 19-44 under 35 U.S.C. § 103 as being unpatentable over Reader et al. (U.S. Patent No. 6,192,073) in view of Kim (U.S. Patent No. 5926,187), further in view of Kusters (U.S. Patent No. 5,819,112). In paragraph 11 of the Office Action, the Examiner has alternatively rejected claims 19-44 under 35 U.S.C. § 103 as being unpatentable over Reader et al. in view of Kim.

Applicants respectfully disagree with the Examiner's contentions and submit the following remarks in response.

Applicants note that the Kusters reference U.S. Patent No. 5,819,112 has been incorrectly numbered throughout the Office Action as "U.S. Patent No. 5,519,112." Appropriate acknowledgement and correction is requested.

As noted in prior amendments both independent claims 19 and 28 include the limitation of a data streamer, coupled to the data transfer switch, and configured to schedule simultaneous data transfers among a plurality of modules disposed within the multimedia processor, at least one of which is a cache memory, in accordance with corresponding channel allocations.

In this configuration, the present invention maintains a data streamer 122 which provides advantages over prior art systems in that it maintains the ability to *schedule data transfers* among a plurality of modules disposed within the multimedia processor by means of simultaneously establishing connections with a plurality of modules in accordance with the corresponding channel allocations. See pages 37-44 of the specification. To this end, the data

F

streamer implements a pipelined logic to handle its buffers and manage the reading and writing of data into the data streamer buffer memory. Such an arrangement increases data transfer efficiency and further increases the processing efficiency of the processor.

As such, in addition to standard buffered data movements within the multimedia processor, the data streamer 122 of the present invention is also capable of scheduling data transfers as well.

Turning to the rejections of independent claims 19 and 28, the cited prior art, namely Reader, teaches a method and apparatus for processing video data using three processors capable to operate concurrently; a scaler processor, a vector processor and a bit stream processor. Reader provides for a vector coprocessor 220 that performs linear transformation and bitstream processor 245 that encodes/decodes input/output data to or from the vector processor 220 to perform distributed processing of multiple data streams.

In particular, as illustrated in Fig. 2 of Reader, bitstream processor 245 is coupled to IO BUS 240 and thus is connected to vector coprocessor 220 and scalar processor ARM7 RISC CPU 210. As discussed in column 5, lines 4-36 of Reader, bitstream processor 245 r*eceives data from vector compressor 220* via IO BUS 240 and cache subsystem 230, *and transfers an operation result to scalar processor (CPU 210)* via IO BUS 240 and cache subsystem 230.

In particular, column 5, lines 11-14 state:

> "Bitstream processor 245 receives the output of VP 220 and produces GOBs (Groups of Blocks) or slices. In particular, BP 245 *performs Huffman and RLC encoding and zig-zag bitstream processing.*" (emphasis added)

Furthermore, column 5, lines 25-28 state:

> "The resulting GOBs or slices are provided to bitstream processor 245. Processor 245 *performs zig-zag processing and Huffman and RLC decoding*." (emphasis added)

Given these descriptions for the bitstream processor 245 in Reader, it appears that its complete functionality amounts to a mere arithmetic processor, encoding data from the vector processor and delivering the encoded data to the scalar processor.

The cited prior art, namely Kim discloses a video overlay system including a bus device having a processor, a local memory, a video interface and a DMA unit. In Kim, a bitstream processor 246 is employed similar to that disclosed in Reader, which is coupled to a control circuit 280.

The cited reference, namely Kusters is directed to an apparatus for controlling an I/O port by queuing requests and, in response to a predefined condition, enabling the I/O port to receive the interrupt request.

The Examiner contends that one of ordinary skill in the art could combine the references to arrive at the present invention as claimed in the independent claims 19 and 28. In the Office Action, the bitstream processor 245 of Reader is relied on by the Examiner as a prior art example of the data streamer 122 of the present invention, combining such an element with connectivity teachings found in Kim.

However, such an equating of the bitstream processor 245 of Reader to the data streamer 122 of the present invention is in error. As discussed above, the data streamer 122 of the present

F

invention is capable not only of transferring data within the multimedia processor, but it also *schedules* simultaneous data transfers among a plurality of modules disposed within the multimedia processor. There is no indication in Reader that its bitstream processor 245 or the corresponding bit stream processor 246 in Kim is capable of such scheduling tasks. Rarther, as pointed out above, the bitstream processor 245 of Reader is merely an arithmetic processor for performing simple encoding and decoding functions. Such, encoding and decoding functions are not analogous to scheduling functions, as they do not require the use of a scheduling logic, such as that employed by the present invention data streamer 122.

As such, there is no teaching or suggestion in any of the cited prior art references, either alone or in combination with one another, that disclose the data streamer of the present invention. For example, there is no teaching or suggestion in Reader or in any of the other cited prior art that discloses a data streamer, configured to *schedule simultaneous data transfers among a plurality of modules* disposed within the multimedia processor.

Likewise, even if the cited references, Reader, Kim, and Kusters were combined, the resulting structure would still not contain all of the elements of the present invention as claimed in independent claims 19 and 28. For example, the resulting structure would still not teach or suggest a data streamer, configured to schedule simultaneous data transfers among a plurality of modules disposed within the multimedia processor.

In view of the forgoing, Applicants respectfully request that the rejection of independent claims 19 and 28 be withdrawn. Additionally, for the same reasons set forth above, Applicants

F

also request that the rejection of claims 20-27 and 29-44, which depend therefrom also be withdrawn.

As such, Applicants respectfully submit that the present invention as claimed is now in condition for allowance, the earliest possible notice of which is earnestly solicited. If the Examiner feels that a telephone interview would advance the prosecution of this application he is invited to contact the undersigned at the number listed below.

Respectfully submitted

SOFER & HARON, LLP

Dated: 1/20/04 By: _____

Joseph Sofer
Reg. No. 34, 438
317 Madison Avenue
Suite 910
New York, New York 10017
(212)697-2800

F